We Claim:

1. A decoding apparatus, comprising:

at least one turbo-decoding and Viterbi-decoding decoder having:

at least one first Viterbi-decoding data path for Viterbi decoding of a convolution code; and

at least one second turbo-code data path for decoding of a turbo code; and

a common memory connected to said decoder and having a multiplicity of individual memory areas, at least one of said memory areas being allocated through said first Viterbi-decoding data path in a Viterbi mode and through said second turbo-code data path in a turbo mode.

2. The decoding apparatus according to claim 1, wherein said common memory has a memory size configured with respect to a required memory size for turbo decoding.

3. The decoding apparatus according to claim 1, wherein said decoder has data paths formed in hardwired logic.

4. The decoding apparatus according to claim 1, wherein said first data path is a hard output Viterbi algorithm decoding data path.

5. The decoding apparatus according to claim 1, wherein said first data path is an exact hard output Viterbi algorithm decoding data path.

6. The decoding apparatus according to claim 1, wherein said first data path is a soft output Viterbi algorithm decoding data path configured to soft output Viterbi algorithm decode.

7. The decoding apparatus according to claim 1, wherein said second data path is a log MAP mode data path operated in a log MAP mode as part of the turbo code decoding.

8. The decoding apparatus according to claim 1, wherein said second data path is a MAX log MAP mode data path operated in a MAX log MAP mode as part of the turbo code decoding.

9. The decoding apparatus according to claim 1, wherein said first and second data paths have at least one jointly utilized element and said jointly utilized element is an ACS unit.

10. The decoding apparatus according to claim 1, wherein:

wherein said first and second data paths have jointly utilized elements; and

at least one of said jointly utilized elements is a branch metric unit for transition metric determination.

11. The decoding apparatus according to claim 1, wherein said memory has at least one jointly utilized soft input data memory area for storing soft input data.

12. The decoding apparatus according to claim 1, wherein:

said first and second data paths have jointly utilized elements; and

at least one of said jointly utilized elements is a branch metric unit for transition metric determination.

13. The decoding apparatus according to claim 1, wherein said memory has at least one jointly utilized memory area and said jointly utilized memory area stores at least one of traceback values and state metrics.

14. The decoding apparatus according to claim 13, wherein said traceback values are of a trellis diagram and said

traceback values of an entirety of said trellis diagram are stored in said jointly utilized memory area.

15. The decoding apparatus according to claim 1, wherein said memory has at least one jointly utilized log likelihood ratio data memory area for storing log likelihood ratio data from the turbo decoding.

16. The decoding apparatus according to claim 1, further comprising a control device connected to at least one of said decoder and said memory, said control device being programmed to define an operating mode of the decoder and thereby control decoding through said first data path through said second data path.

17. The decoding apparatus according to claim 1, further comprising a control device connected to at least one of said decoder and said memory, said control device being programmed to define an operating mode of the decoder in which decoding through said first data path is effected through said second data path.

18. The decoding apparatus according to claim 1, further comprising a control device connected to said decoded and being programmed to:

define an operating mode of said decoder; and

perform a memory division defined beforehand for a respective operating mode.

19. The decoding apparatus according to claim 17, wherein at least one of said control device and said memory one of:

has a multiplexer; and

performs the functionality of a multiplexer.

20. The decoding apparatus according to claim 18, wherein at least one of said control device and said memory one of:

has a multiplexer; and

performs the functionality of a multiplexer.

21. The decoding apparatus according to claim 19, wherein at least one of said multiplexer and said control device are formed in hardwired logic and are part of the decoder.

22. The decoding apparatus according to claim 20, wherein at least one of said multiplexer and said control device are formed in hardwired logic and are part of the decoder.

23. The decoding apparatus according to claim 17, wherein said control device has a program-controlled unit having a multiplexer functionality.

24. The decoding apparatus according to claim 23, wherein said program-controlled unit is one of a microcontroller and a microprocessor.

25. The decoding apparatus according to claim 18, wherein said control device has a program-controlled unit having a multiplexer functionality.

26. The decoding apparatus according to claim 25, wherein said program-controlled unit is one of a microcontroller and a microprocessor.

27. The decoding apparatus according to claim 17, wherein said memory has a memory area occupancy fixedly prescribed for a respective one of said data paths through said control device.

28. The decoding apparatus according to claim 18, wherein said memory has a memory area occupancy fixedly prescribed for a respective one of said data paths through said control device.

29. The decoding apparatus according to claim 1, wherein said decoder is at least partially formed in hardware.

30. The decoding apparatus according to claim 1, wherein said decoder is at entirely formed in hardware.

31. A decoding apparatus, comprising:

at least one turbo-decoding and Viterbi-decoding decoder having:

a first data path for Viterbi decoding a convolution code; and

a second data path for turbo-code decoding of a turbo code; and

said first data path and said second data path having at least one common portion decoding data both in a turbo-code decoding mode and in a Viterbi decoding mode.

32. The decoding apparatus according to claim 31, further comprising a common memory connected to said decoder and having a multiplicity of individual memory areas, at least one of said memory areas being allocated through said first

Viterbi-decoding data path in the Viterbi mode and through said second turbo-code data path in the turbo mode.

33. The decoding apparatus according to claim 32, wherein said common memory has a memory size configured with respect to a required memory size for turbo decoding.

34. The decoding apparatus according to claim 31, wherein said decoder has data paths formed in hardwired logic.

35. The decoding apparatus according to claim 31, wherein said first data path is a hard output Viterbi algorithm decoding data path.

36. The decoding apparatus according to claim 31, wherein said first data path is an exact hard output Viterbi algorithm decoding data path.

37. The decoding apparatus according to claim 31, wherein said first data path is a soft output Viterbi algorithm decoding data path configured to soft output Viterbi algorithm decode.

38. The decoding apparatus according to claim 31, wherein said second data path is a log MAP mode data path operated in a log MAP mode as part of the turbo code decoding.

39. The decoding apparatus according to claim 31, wherein said second data path is a MAX log MAP mode data path operated in a MAX log MAP mode as part of the turbo code decoding.

40. The decoding apparatus according to claim 31, wherein said first and second data paths have at least one jointly utilized element and said jointly utilized element is an ACS unit.

41. The decoding apparatus according to claim 31, wherein:

wherein said first and second data paths have jointly utilized elements; and

at least one of said jointly utilized elements is a branch metric unit for transition metric determination.

42. The decoding apparatus according to claim 32, wherein said memory has at least one jointly utilized soft input data memory area for storing soft input data.

43. The decoding apparatus according to claim 31, wherein:

said first and second data paths have jointly utilized elements; and

at least one of said jointly utilized elements is a branch metric unit for transition metric determination.

44. The decoding apparatus according to claim 32, wherein said memory has at least one jointly utilized memory area and said jointly utilized memory area stores at least one of traceback values and state metrics.

45. The decoding apparatus according to claim 44, wherein said traceback values are of a trellis diagram and said traceback values of an entirety of said trellis diagram are stored in said jointly utilized memory area.

46. The decoding apparatus according to claim 32, wherein said memory has at least one jointly utilized log likelihood ratio data memory area for storing log likelihood ratio data from the turbo decoding.

47. The decoding apparatus according to claim 32, further comprising a control device connected to at least one of said decoder and said memory, said control device being programmed to define an operating mode of the decoder and thereby control decoding through said first data path through said second data path.

48. The decoding apparatus according to claim 32, further comprising a control device connected to at least one of said decoder and said memory, said control device being programmed to define an operating mode of the decoder in which decoding through said first data path is effected through said second data path.

49. The decoding apparatus according to claim 32, further comprising a control device connected to said decoded and being programmed to:

define an operating mode of said decoder; and

perform a memory division defined beforehand for a respective operating mode.

50. The decoding apparatus according to claim 48, wherein at least one of said control device and said memory one of:

has a multiplexer; and

performs the functionality of a multiplexer.

51. The decoding apparatus according to claim 49, wherein at least one of said control device and said memory one of:

has a multiplexer; and

performs the functionality of a multiplexer.

52. The decoding apparatus according to claim 50, wherein at least one of said multiplexer and said control device are formed in hardwired logic and are part of the decoder.

53. The decoding apparatus according to claim 51, wherein at least one of said multiplexer and said control device are formed in hardwired logic and are part of the decoder.

54. The decoding apparatus according to claim 48, wherein said control device has a program-controlled unit having a multiplexer functionality.

55. The decoding apparatus according to claim 54, wherein said program-controlled unit is one of a microcontroller and a microprocessor.

56. The decoding apparatus according to claim 49, wherein said control device has a program-controlled unit having a multiplexer functionality.

57. The decoding apparatus according to claim 56, wherein said program-controlled unit is one of a microcontroller and a microprocessor.

58. The decoding apparatus according to claim 48, wherein said memory has a memory area occupancy fixedly prescribed for a respective one of said data paths through said control device.

59. The decoding apparatus according to claim 49, wherein said memory has a memory area occupancy fixedly prescribed for a respective one of said data paths through said control device.

60. The decoding apparatus according to claim 31, wherein said decoder is at least partially formed in hardware.

61. The decoding apparatus according to claim 31, wherein said decoder is at entirely formed in hardware.

62. A decoding apparatus, comprising:

at least one decoder configured to decode both by turbo-decoding and by Viterbi-decoding, said decoder having:

at least one first Viterbi-decoding data path for Viterbi decoding of a convolution code; and

at least one second turbo-code data path for decoding of a turbo code; and

a common memory connected to said decoder and having a multiplicity of individual memory areas, at least one of said memory areas being allocated through said first Viterbi-decoding data path in a Viterbi mode and through said second turbo-code data path in a turbo mode.

63. A decoding apparatus, comprising:

at least one turbo-decoding and Viterbi-decoding decoder having:

a first data path for Viterbi decoding a convolution code; and

a second data path for turbo-code decoding of a turbo code; and

at least parts of said first data path and of said second data path being jointly utilized both for the turbo-code decoding and for the Viterbi decoding.

64. The decoding apparatus according to claim 1, further comprising a trellis processor programmed to:

operate both in a Viterbi decoding mode for a convolution code and in a decoding mode for a turbo code; and

utilize said first and second data paths and areas of said memory at least partially jointly in the Viterbi decoding mode and the turbo code decoding mode.

65. The decoding apparatus according to claim 32, further comprising a trellis processor programmed to:

operate both in a Viterbi decoding mode for a convolution code and in a decoding mode for a turbo code; and

utilize said first and second data paths and areas of said memory at least partially jointly in the Viterbi decoding mode and the turbo code decoding mode.

66. The decoding apparatus according to claim 62, further comprising a trellis processor programmed to:

operate both in a Viterbi decoding mode for a convolution code and in a decoding mode for a turbo code; and

utilize said first and second data paths and areas of said memory at least partially jointly in the Viterbi decoding mode and the turbo code decoding mode.

67. The decoding apparatus according to claim 63, further comprising:

a common memory connected to said decoder and having a multiplicity of individual memory areas, at least one of said memory areas being allocated through said first Viterbi-decoding data path in the Viterbi mode and through said second turbo-code data path in the turbo mode; and

a trellis processor programmed to:

operate both in a Viterbi decoding mode for a convolution code and in a decoding mode for a turbo code; and

utilize said first and second data paths and areas of said memory at least partially jointly in the Viterbi decoding mode and the turbo code decoding mode.

68. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 1; and

implementing:

at least one first decoding utilizing an exact Viterbi algorithm; and

at least one second decoding utilizing one of a MAP algorithm and a turbo code.

69. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 31; and

implementing:

at least one first decoding utilizing an exact Viterbi algorithm; and

at least one second decoding utilizing one of a MAP algorithm and a turbo code.

70. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 62; and

implementing:

at least one first decoding utilizing an exact Viterbi algorithm; and

at least one second decoding utilizing one of a MAP algorithm and a turbo code.

71. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 63; and

implementing:

at least one first decoding utilizing an exact Viterbi algorithm; and

at least one second decoding utilizing one of a MAP algorithm and a turbo code.

72. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 1;

providing a trellis diagram with traceback values; and

storing the traceback values of an entirety of the trellis diagram in the memory.

73. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 31;

providing a trellis diagram with traceback values; and

storing the traceback values of an entirety of the trellis diagram in the memory.

74. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 62;

providing a trellis diagram with traceback values; and

storing the traceback values of an entirety of the trellis diagram in the memory.

75. A method for operating a decoder, which comprises:

providing the decoding apparatus according to claim 63;

providing a trellis diagram with traceback values; and

storing the traceback values of an entirety of the trellis diagram in the memory.